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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,861	05/24/2000	Timothy J. Williams	0325.00339	4837

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 07/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/577,861	WILLIAMS, TIMOTHY J.	
	Examiner	Art Unit	
	Albert Wang	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is responsive to Amendment A filed May 8, 2003, in which claims 1, 4-6, 8, 9, 11, 12, and 14-20 are amend, and new claims 21-25 are added. Claims 1-25 are pending.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-9, 11-19, 21-23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yach et al., U.S. Patent No. 5,454,114 ("Yach"), in view of Choudhury, U.S. Patent No. 6,229,367.

As per claim 1, Yach teaches an apparatus comprising:

a first circuit (Fig. 1, module 15) configured to wake up a second circuit (Fig. 1, CPU) in response to an input signal (Col. 15, lines 3-9).

While Yach does teach a programmable delay (Claim 1, "timer having separately programmable time-out interval"), Yach does not teach expressly the details for an input signal comprising a programmable delay. Choudhury teaches the details of selecting a programmable delay using an input signal (Fig. 3, signal on time delay selector line 900). At the time of the invention, it would have obvious to one skilled in the art to apply the details of Choudhury's using an input signal to select a programmable delay to Yach's apparatus. The motivation for doing would have been to insure the integrity of selecting a programmable delay.

As per claims 2 and 3, Choudhury teaches a user programmable multi-bit input signal (Fig. 1a, delay control bits S0-S3).

As per claim 4, the programmable delay value of Choudhury is inherently in response to one or more firmware instructions. Yach teaches firmware (on microcontroller chip 10).

As per claim 5, Yach teaches a wake-up delay timing value (Claim 1, "timer having separately programmable time-out interval").

As per claim 6, Choudhury teaches a first circuit (Fig. 3) comprising:

a delay circuit configured to present a first delay signal (one-shot unit 200); and

a select circuit (comprising multiplexer 400) configured to present a second delay signal (412) in response to said first delay signal and said input signal.

As per claim 7, Choudhury teaches said input signal is configured to control a programmable delay of said second delay signal (Fig. 3, signal on time delay selector line 900).

As per claim 8, Choudhury teaches said programmable delay comprising a multiple of a delay of said first delay signal (Fig. 3, provided by shift register 600).

As per claim 9, Choudhury teaches said select circuit is further configured to select one of a plurality of third delay signals (Fig. 3, from nodes 312-342) in response to said input signal.

As per claim 11, Yach teaches counters said select circuit comprises a counter (Fig. 8, ripple counter).

As per claim 12, Choudhury teaches said delay circuit is further configured to present said first delay signal in response to an enable signal (Fig. 3, input signal 100).

As per claim 13, Choudhury teaches said input signal is generated in response to a device selected from the group consisting of input pins, data pins, microprocessor code, and firmware (Fig. 1a, delay control bits S0-S3).

As per claim 21, Yach teaches said first and second circuits are implemented on a single integrated circuit (Fig. 1, microcontroller chip 10).

As per claim 22, Yach teaches a watchdog timer (Fig. 1, module 15; Col. 13, lines 16-32) that is configured to periodically wake up said second circuit.

As per claim 23, Yach teaches a second circuit (Fig. 1, CPU) that is capable of generating said input signal.

As per claims 14 and 25, since Yach/Choudhury teaches the apparatus of claims 1-9, 11-13 and 21-23, the combination teaches the claimed apparatus.

As per claims 15-19, since Yach/Choudhury teaches the apparatus of claims 1-9, 11-13 and 21-23, the combination teaches the claimed method.

3. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yach/Choudhury, as applied to claims 1 and 6 above, further in view of Kinget et al., U.S. Patent No. 6,281,721 ("Kinget").

As per claim 10, while Choudhury teaches functionally equivalent circuits using delay elements and multiplexers (Figs. 1a & 14a; Col. 1, lines 32-42), Yach/Choudhury does not expressly teach using dividers as delay elements. Kinget teaches a circuit using divider elements and multiplexers (Fig. 1). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the Kinget's dividers to Choudhury's circuit because such application would have bee a matter of design substitution.

4. Claims 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yach/Choudhury, as applied to claims 1 and 6 above, further in view of Lee et al., U.S. Patent No. 6,025,745 ("Lee").

As per claims 20 and 24, Yach/Choudhury does not expressly teach calibrating a programmable delay circuit. Lee teaches the steps for calibrating a delay circuit (Fig. 3). At the time of the invention, it would have been obvious to one of ordinary skill in the art to Lee's calibrating to Yach/Choudhury's method in order to adjust delay to account for variations such as those due to variations in environment and manufacture.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

aw
July 21, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100